

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
22 April 2004 (22.04.2004)

PCT

(10) International Publication Number
WO 2004/034652 A1

(51) International Patent Classification⁷: **H04L 12/56**,
29/06, 12/28

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Philips Intellectual
Property & Standards, Prof. Holstlaan 6, NL-5656 AA
Eindhoven (NL).

(21) International Application Number:
PCT/IB2003/004401

(22) International Filing Date: 7 October 2003 (07.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02079196.8 8 October 2002 (08.10.2002) EP
03101095.2 22 April 2003 (22.04.2003) EP

(71) Applicant (for all designated States except US): **KONIN-
KLJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **RADULESCU, An-
drei** [RO/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eind-
hoven (NL).

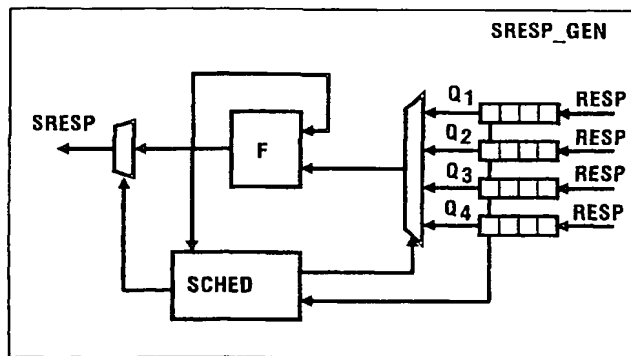
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE,
GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR,
KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK,
MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT,
RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT AND METHOD FOR ESTABLISHING TRANSACTIONS

NI



(57) Abstract: An integrated circuit (IC) comprises a network and a plurality of modules (M1, M2, M3) which communicate to each other via the network. A first module (M1) sends a plurality of requests (REQ) to at least two second modules (M2, M3, Mn) and the second modules send individual responses (RESP2, RESP3, RESPn) to the first module, indicating a result of the execution of the requests. The integrated circuit (IC) comprises a network capable of sending a single response (SRESP) to the first module (M1) dependent on the individual responses (RESP2, RESP3 up to and including RESPn) from the second modules (M2, M3, Mn). The single response (SRESP) can indicate that at least one second module has executed the requests (REQ) or that a specific error has occurred in at least one of the second modules (M2, M3, Mn). The single response (SRESP) can also indicate which types of error have occurred in the second modules (M2, M3, Mn). If various errors have occurred, the single response (SRESP) can indicate which error is the most serious error or information about all errors.

WO 2004/034652 A1